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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,923	01/17/2001	Yun-Kuei Yang	JCLA6211	5550

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J.C. PATENTS INC.
Suite 250
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EXAMINER

VINH, LAN

ART UNIT	PAPER NUMBER
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1765

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DATE MAILED: 11/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/761,923

Applicant(s)

YANG ET AL.

Examiner

Lan Vinh

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-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al (US 6,326,300) in view of Violette (US 6,140,244)

Liu discloses a method of forming dual damascene patterned conduction layer.

This method comprises the steps of:

forming a substrate 10 (col 7, line 8)

forming a first dielectric layer 12 on the substrate 10, the dielectric layer is implanted with dopant (col 7, lines 9-10; col 13, lines 26-27)

forming a undoped dielectric layer 22 (silicon oxide) on the doped dielectric layer 12 (col 9, lines 33-34; fig. 4)

forming a patterned photoresist layer/mask 24 on the dielectric layer 22 (col 9, lines 20-21; fig. 4 of Liu shows that patterned photoresist layer/mask 24 has an opening/first opening exposing a portion of the dielectric layer 22

implanting the masked undoped dielectric layer 22 to form a ion implanted region/doped region in a portion of the exposed dielectric layer 22 below the opening in the mask 24/first opening (col 10, lines 48-51; fig.5)

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etching the masked undoped dielectric layer 22 to remove the ion implanted region/doped region to form a second opening exposing a portion of the dielectric layer 22 below the implanted/doped region (col 11, lines 16-20; fig. 5)

performing a second etching step on the masked undoped dielectric layer 22 to remove a portion of the dielectric layer 22 under the implanted/doped region and a portion of dielectric layer 12/doped dielectric layer to expose a portion of the substrate 10 (col 11, lines 25-30; fig. 6)

Unlike the instant claimed invention as per claims 1 and 11, Liu does not specifically disclose performing a chemical vapor etching step with HF on the masked undoped dielectric layer to remove the implanted/doped region having a depth that does not exceed a thickness of the undoped dielectric layer.

However, Violette discloses a method for forming a dielectric structure comprises the step of performing a chemical vapor etching step with HF to remove the implanted/doped region 18 having a depth that does not exceed a thickness of the undoped dielectric layer 16 (col 3, lines 51-53; col 4, lines 1-5 and fig.5)

Since both Liu and Violette are concerned with method of etching to remove a implanted/doped region in a dielectric layer (oxide), one skilled in the art would have found it obvious to modify Liu's step of etching the masked undoped dielectric layer 22 to remove the ion implanted/doped region by using a vapor etching step with HF to remove the implanted/doped region as per Violette because Violette teaches that HF/HF vapor etch removes doped silicon dioxide at a faster rate than undoped silicon

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oxide allowing the formation of specialized silicon dioxide/dielectric structure and HF based etchant will not harm silicon substrate (col 3, lines 52-58; col 4, lines 15-16)

Regarding claims 2-4, Liu discloses that the dielectric layer is TEOS (col 13, lines 11-13), doping the dielectric with boron and phosphorus (col 13, table 1)

Regarding claim 5, Liu discloses that doped dielectric layer 12 may be formed by silicon nitride (col 7, lines 13-17)

Regarding claim 6-7, Liu discloses that the undoped dielectric layer 22 includes silicon oxide and silicon nitride layer (col 9, lines 41-43)

Regarding claims 8-10, Liu discloses implanting the undoped dielectric layer 22 below the opening in the mask 24 with boron, phosphorous and arsenic (col 8, lines 54-57)

Regarding claim 12, fig. 5 of Liu shows that the thickness of the implanted region/doped region is more than 70%/ at least 70% of the thickness of doped dielectric layer 12

Regarding claim 13, fig. 6 of Liu shows that the thickness of the second opening is more than the thickness of the undoped dielectric layer 22 which reads on the thickness of the second opening is at least 70% of the thickness of the undoped dielectric layer

The limitation of claim 14 has been discussed above

Regarding claim 15, Liu discloses the step of removing the patterned photoresist/mask after etching (col 12, lines 34-36)

3. Claims 16, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al (US 6,326,300) in view of Violette (US 6,140,244)

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Liu discloses a method of forming dual damascene patterned conduction layer.

This method comprises the steps of:

forming a substrate 10 (col 7, line 8)

forming a undoped dielectric layer 22 (silicon oxide) on the doped dielectric layer 12 (col 9, lines 33-34; fig. 4)

forming a patterned photoresist layer 24 on the dielectric layer 22 (col 9, lines 20-21; fig. 4 of Liu shows that patterned photoresist layer 24 has an opening/first opening exposing a portion of the dielectric layer 22

implanting the masked undoped dielectric layer 22 to form a ion implanted region/doped region in a portion of the exposed dielectric layer 22 below the opening in the mask 24/first opening (col 10, lines 48-51; fig.5)

etching the masked undoped dielectric layer 22 with the photoresist layer as a mask to remove the ion implanted region/doped region to form a second opening exposing a portion of the dielectric layer 22 (col 11, lines 16-20; fig. 5)

performing a second plasma etching step/dry etching on the undoped dielectric layer 22 using photoresist layer 24 as a mask to remove a exposed portion of the dielectric layer 22 in the second opening to expose a portion of the substrate 10 (col 11, lines 25-30; fig. 6)

Unlike the instant claimed invention as per claim 16, Liu does not specifically disclose performing a chemical vapor etching step to remove the implanted/doped region having a depth that does not exceed a thickness of the undoped dielectric layer.

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However, Violette discloses a method for forming a dielectric structure comprises the step of performing a chemical vapor etching step to remove the implanted/doped region 18 having a depth that does not exceed a thickness of the undoped dielectric layer 16 (col 3, lines 51-53; col 4, lines 1-5 and fig.5)

Since both Liu and Violette are concerned with method of etching to remove a implanted/doped region in a dielectric layer (oxide), one skilled in the art would have found it obvious to modify Liu's step of etching the masked undoped dielectric layer 22 to remove the ion implanted/doped region by using a vapor etching step to remove the implanted/doped region as per Violette because Violette teaches that vapor etch removes doped silicon dioxide at a faster rate than undoped silicon oxide allowing the formation of specialized silicon dioxide/dielectric structure (col 3, lines 52-58)

Regarding claim 18, fig. 5 of Liu shows that the depth of the implanted region/doped region is more than 50%/ at least 50% of the thickness of doped dielectric layer 12

Regarding claim 19, fig. 6 of Liu shows that the depth of the second opening is more than the thickness of the undoped dielectric layer 22 which reads on the thickness of the second opening is at least 50% of the thickness of the undoped dielectric layer.

4. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al (US 6,326,300) in view of Violette (US 6,140,244) and further in view of McDaniel et al (US 6,350,679)

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Liu as modified by Violette has been described above in paragraph 2. Liu and Violette differs from the instant claimed invention as per claim 17 by performing the chemical vapor etching using HF instead of hydrophosphoric

However, McDaniel, in a method of providing interlevel dielectric layer, teaches that dielectric layer can be etched using wet etching such as HF, phosphoric acid (col 4, lines 50-52)

Hence, one skilled in the art would have found it obvious to modify Liu and Violette step of chemical etching step by using hydrophosphoric vapor etching step in view of McDaniel teaching because both HF and phosphoric are known etching solution to remove dielectric material, thus the substitution of one for the other would have produced an expected result.

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Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302.

The examiner can normally be reached on M-F 8:30-5:30.PM

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.



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LV
November 5, 2002